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Design an 20-Bit, 20 MS/s Pipeline ADC on 90nm CMOS with 154.57dB SFDR

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***Abstract*—**This paper introduces innovative high-speed, high-resolution pipeline ADC architecture, designed with a 1.8V supply voltage and simulated using 90nm CMOS technology in Cadence. The proposed design achieves a 20-bit resolution with a sampling rate of 20 MS/s while maintaining an efficient power consumption of 16.7mW. Operating at a 1 kHz input frequency, this converter is particularly well-suited for biomedical monitoring systems. Performance metrics reveal impressive results: 154.57 dB spurious-free dynamic range (SFDR), 18.75 effective number of bits (ENOB), and differential non-linearity (DNL) values ranging from -0.18 LSB to +0.4 LSB. The design maintains exceptional power efficiency, consuming only 16.7mW at 1.8V supply voltage. These characteristics position our ADC as an excellent choice for both biomedical instruments and precision measurement systems requiring high-resolution signal conversion.

***Index Terms*— Pipeline ADC, CMOS, Op-amp, S/H circuit, Folded Op amp cadence Tool.**

I. INTRODUCTION

Recent developments in low-power circuitry design, communication techniques, and CMOS technologies have sparked a great deal of interest in individual health devices for monitoring. The biomedical acquiring system consists of a radio frequency (RF) transceiver, microcontroller, sensor, analog front-end amplifier, and ADC, is one of the key parts of these systems. In order to transform analog information into digital signals for the biomedical acquisition system, the ADC is essential. The characteristics of biological signals are depicted in figure 1 [1]. For example, in ECG applications, the dynamic range that is need can reach up to 60 dB, which means that the ADC has to have a resolution of about 10 bits. Nonetheless, an 8-bit resolution is usually adequate for ECG applications. The requirements for a sequential analog-to-digital converter (SAR ADC) with low power consumption, moderate speed, and high resolution capabilities are highlighted by these features of biological signals.

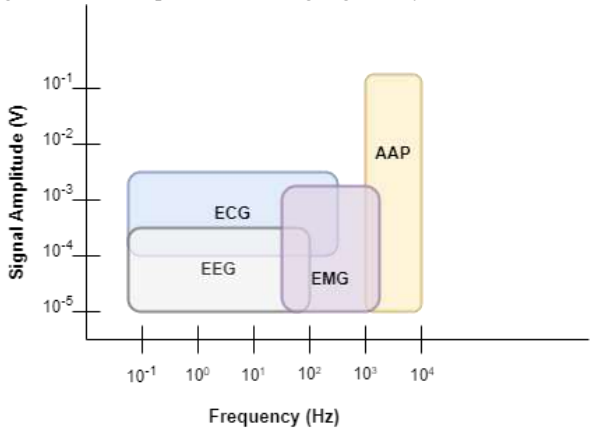

Figure 1.Characteristics of biomedical signals

The work in [1] imposes the energy efficient and fully differential technique used for 8,12 bits ADC for data acquisition in health related system, this technique provides low power. The whole architecture was implemented on 180 nm CMOS technology. By using weak inversion region based transition in [2], design of 8 bit pipeline ADC was implemented on 130nm CMOS process for low power. Switching technique was used for 8 bit SAR ADC with low power circuit and implemented on 180 nm CMOS technology in [3]. The 9 bit SAR ADC was designed by a novel architecture in [4] without using op amp, reducing capacitance from 512c to 64c and implemented on 65nm CMOS technology.Design of 10 bit ADC with energy efficient low complexity switching technique was achieved by work done in [5] resulting in low power. Novel architecture for low power dynamic comparator based 10 bit SAR ADC was designed for biomedical application with low power and implemented on 65 nm CMOS technology with the 1 KS/s sampling rate in [6].Study in [7] shows Energy efficient Vcm based switching technique used to design 10 bit SAR ADC for reducing power consumption and area occupation. Sampling rate of ADC was 120KS/s and implemented on 180 nm CMOS technology.

A complete monolithic 16-bit, 1 MS/s, low-power ADC with low power & high speed are acquired using a pipelined architecture. A 32-bit on-chip customized microcontroller calibrates and corrects the pipeline linearity between 0.75 LSB INL and 0.6 LSB DNL [8], Another similar work [9] reported a 16-bit ADC is designed using a high-performance complementary BJTs and complementary SiGe Bi CMOS SOI process. The research in [10] shows a 16-bit pipelined ADC designed for low power with simulated result SFDR and SNDR to be 91.9dB and 7402dB respectively, 210mW is power consumption at sampling rate 100 MS/s. The work in [11-12] presents a modified gain CMOS Operational OTA technique used for a 16 bit pipeline ADC designed for achieving 161 MHz bandwidth. A new formula for high concerning sampling rate and linearity is established for design 16 bit and 200 MS/s pipeline ADC model in [13]. A Novel "Split ADC" Architecture based design as well as fabrication of a 16-bit Pipeline ADC using 0.25 μm CMOS is proposed in [14]. In [15], 16 bits Pipeline ADC is designed using external reference voltage scheme for sampling rate 200 MS/s.

The work in [16] presents the power analysis and optimization for the speed and for high-resolution designed 16-bit 200MS/s pipeline ADC. The systematic level design technique for low-power is used. Results of simulation assure less than 700mW consumption of core ADC. A design method used for inter stage gain schemes that retains all the proceeds of traditional schemes and hence optimizes power consumption is displayed in [17]. A prototype of 16-bit 20 Ms/s ADC with a required power consumption of 200mW is designed using these schemes. The study in [18] presents a 16-bit, 250 MS/s Digital Signals Defrayer (ADC) with a new technique of linearization which minimize distortion, the power consumption reduction by 70% and achieves SNDR of 76.5dB from a supply of 1.8 V.

An 8 bit pipeline IADC is designed in [19] by current mode technique which can be operated at 4.5 MSPS with SNDR of 51dB. The design in [20] displays a "split reference" regulation technique used for pipelined ADC which operates within 1 MS/s and 1 GS/s. The authors in [21] designed a 100-MS/s double-channel pipeline structure using op-amp sharing scheme designed with memory effect cancellation technique is described that diminishes cross coupling among channels and improves linearity. Implementation of a 12-bit and 14 bit pipelined digital data control fabricated on 40 nm TSMC technology is aimed in [22] to minimize the power through residue amplifiers and comparator cells for achieved sampling rate 500 MS/s. The work in [23] uses ACLS and RS, proposes an ADC design that acquires a SNDR and SFDR 74.3-dB and 85.5-dB respectively and it consumes 5.1mW power. A new massive dither injection technique is described in [24] to enhance pipeline linearity of

ADC for high resolution and speed. The authors in [25] reported a high-speed front-end circuit applied in an ADC. It shows SFDR greater than 95dB for sinusoidal input being 25.39-MHz at 2Vpp.

The work in [26] reported two 6-bit pipelined current-mode ADCs providing high speed and resolution along with minimum power designed and simulated on 0.18um-UMC MM (Mixed-Mode) CMOS process. As a result, sampling rate is 50MS/s, average power dissipation 56.38mW & SNR is 36.33dB, respectively. Study in [27] shows a 2-bit/stage Multiplying DAC (MDAC) giving a 7-bit 16MS/s CMOS pipeline ADC for Zig Bee receiver application is devised to in the mentioned paper. Dissipated power is 3.7mW from a 1.8-V supply. The paper in [28] proposes an architecture displaying a new 2-stage architecture ADC, which uses a customized pipeline dependent on Successive-Approximation ADCs. ADC designed in [29] shows a 3-stage pipeline based on β-expansion at every pipeline stage is a non-binary cycle. This prototype acquires a 61.07dB SNDR at 10MS/s. Authors of [30] shows a chip with a 25GHz-fT complementary SOI BiCMOS based ADC generating a 80.1dBFS SNR, 98dBc SFDR at 2MHz. The area of 5x5.3mm2 that consumes power is 1.7W.

Displays a smart methodology to simulate INL and Spice that permits implementation of Sample/Hold with low-distortion and quantizes and provides greater input range. Correctly predicting the aperture uncertainty allows the optimization of the on-chip clock circuit to yield l80fs RMS jitters and 73.5dBFS SNR at 150MHz input [31-32].Proposes a 16 channel, 14 bit, 50MS/s calibration free pipeline SAR ADC designed for ultrasound application. Pesudo differential pipeline ADC has been designed by investing techniques like nested CMOS gain boosting and a passive capacitor error averaging for 14 bit and 12 MS/s sample rate for low power application [33-34].

As the number of bits increases in the pipeline ADC, the number of stages also increases as we move from lower to higher bit resolution in the ADC

The proposed design solves all the limitations discussed earlier. The major contribution of the work follows:

- The design of a 4-bit flash ADC is based on a novel architecture op-amp, which is limited to four inputs and two outputs.
- The proposed 20-bit design of pipeline ADC reduced the number of stages compared to the conventional design.
- The proposed 20-bit pipeline ADC design shows better performance in terms of SFDR, SNR, ENOB and DNL.

II. PROPOSED METHODOLOGY

The proposed 20-bit Pipeline ADC is implemented on a 90nm CMOS process for achieving 20 MS/s sampling rate as shown in figure 2. Mentioned architecture is built in 7 stages with 4 bit per stage as shown in Figure 2. Pipelining is fast as compared to parallel architecture. The concurrent operation of the stages happens at any time. The recent available sample works on every stage of ADCs. The residues left over by the previous sample works on later stages. The output digital data is ready on every clock cycle after the pipeline is primed. The proposed architecture includes 4-bit DAC, 4-bit Flash ADC, sample & hold block and a residue amplifier at each stage the power consumed is 553.8uW by each stage and hence the total consumed power is 16.7mW for the complete 20-bit pipeline ADC. The proposed diagram of single stage 4-bit pipeline ADC is displayed in figure 3.

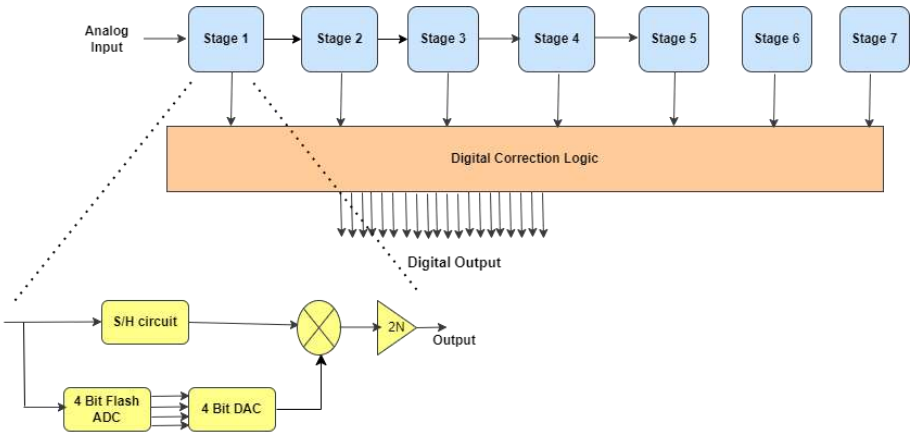

Figure 2.Proposed architecture of Pipeline ADC

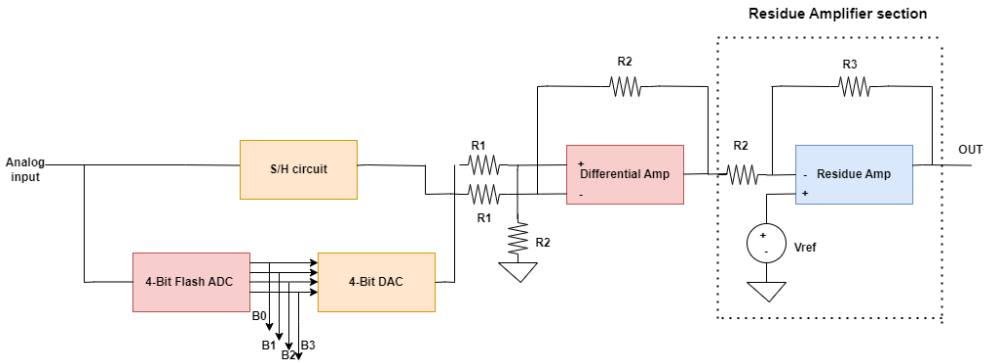

Figure 2. Detail diagram of proposed 4 bit pipeline ADC

II.A SAMPLE AND HOLD CIRCUIT

This circuit is a fundamental component in the given pipelined ADC architecture. The circuit, illustrated in Figure 4, is designed to operate at twice the conventional sampling rate, thereby enhancing the overall conversion speed. The sampling mechanism is implemented using a parallel combination of two NMOS transistors (M1 and M2), cascoded with an additional NMOS transistor (M3). The incorporation of this parallel-cascode structure effectively increases the on-resistance (R_{on}) and overall gain, that ultimately improves the speed and efficiency of the sampling process. The circuit employs three capacitors (C_{s1}, C_{s2} and C_L), which facilitate the charge and discharge operations during the sampling and holding phases. A 1 pF loading capacitor (C_L) is integrated at the output to stabilize the sampled voltage. The sinusoidal input signal excites the transistors' source nodes, while a control pulse is provided at the gate of the inverter stage to regulate the sampling operation. The parallel NMOS configuration increases the drain current (I_D), enabling the capacitors to charge up to the input voltage (V_{in}).Although this circuit is capable of operating at a sampling rate of 500 MS/s, it has been optimized for 20 MS/s in the proposed pipeline ADC architecture, as illustrated in Figure 5.

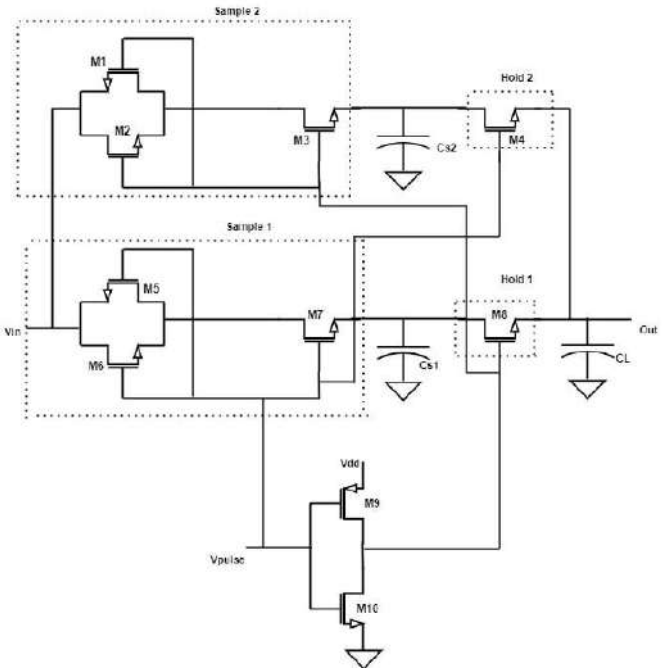

Figure 3.Schematic view of S/H circuit

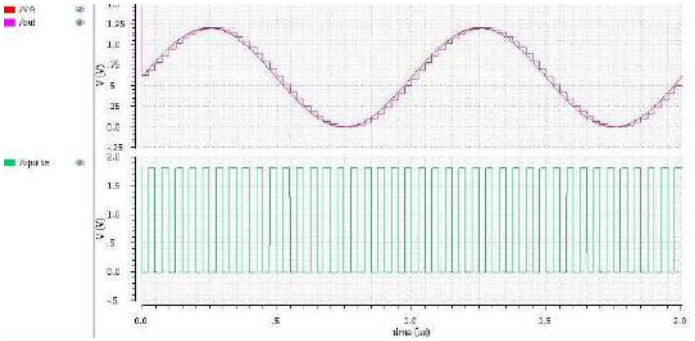

Figure 4.Simulation view of S/H circuit

II.B 4-BIT FLASH ADC

The implemented flash analog-to-digital converter (ADC) functions as a critical sub-component within the proposed pipelined architecture, executing parallel quantization of analog inputs into corresponding digital codes. While flash ADCs demonstrate superior conversion speeds compared to other architectures, their hardware overhead presents notable design constraints. A fundamental limitation emerges from their comparator scaling requirement, where an n-bit resolution necessitates 2^n-1 comparators. This exponential relationship between resolution and comparator count introduces substantial challenges in power efficiency and circuit integration. The increased number of comparators not only elevates static power dissipation but also compounds parasitic effects, thereby impacting the overall system performance..

To address this limitation, a 4-bit flash ADC with a novel operational amplifier (Op-Amp) architecture is proposed. This design incorporates an Op-Amp with four inputs and two outputs, significantly reducing the number of operational amplifiers required compared to conventional flash ADC implementations. Typically, a 4-bit flash ADC requires 15 comparators (2^4-1); however, the proposed design optimizes the comparator arrangement, reducing the requirement to only 8 comparators, as illustrated in Figure 6. This optimization enhances power efficiency and reduces circuit complexity while maintaining high-speed performance.

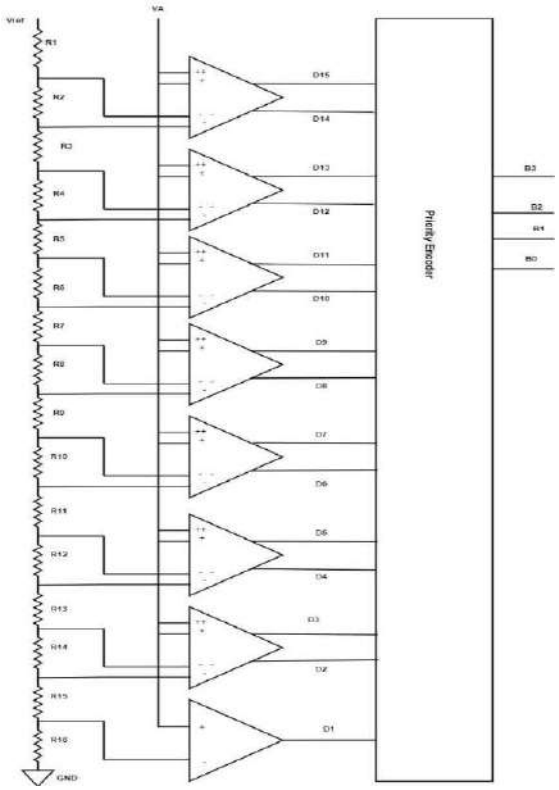

Figure 5.Schematic diagram of 4 Bit Flash ADC

The digitally represented signal is defined in equation (1):

$$code\,for\,digtal = \frac{V_A}{V_{ref}} \times (2^n - 1) \qquad (1)$$

Where,

VA: Analog voltage signal, Vref: reference voltage and n: bit resolution

The accuracy of the digitally represented analog signal improves as the number of output bits increases. A higher-bit resolution allows for finer quantization levels, thereby enhancing signal fidelity. The simulated response of the proposed 4-bit flash ADC is illustrated in Figure 7, presenting the transient simulation results for the four input signals and the corresponding digital output. The simulation confirms the correct functionality of the flash ADC while achieving a low power consumption of 1.7 mW, demonstrating its efficiency in high-speed and low-power applications.

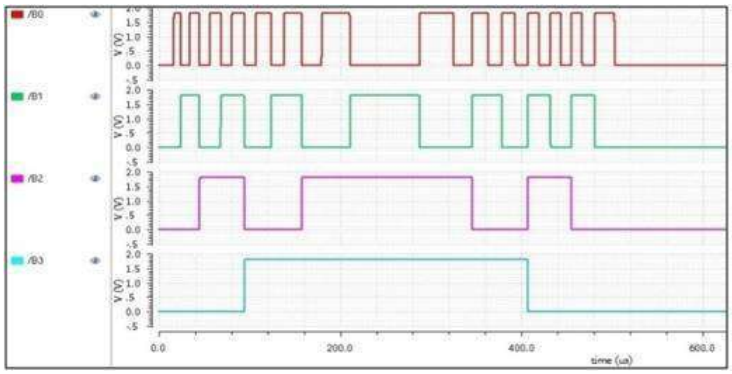

Figure 6.Simulation view of 4 Bit Flash ADC

II.C COMPARATOR AND PRIORITY ENCODER

The comparator architecture implements parallel signal comparison mechanisms, where multiple input voltages are simultaneously evaluated to generate corresponding digital states for subsequent processing by the bit priority encoder. Figure 8 depicts the circuit-level implementation of the proposed operational amplifier (Op-Amp), which serves as the fundamental building block of this multi-input comparison network. This architecture represents a significant departure from conventional two-input comparator designs, offering enhanced functionality within a single comparison stage.

The 4-bit priority encoder receives the complete comparator output and converts it into a binary code based on the highest priority bit. The schematic of the priority encoder is depicted in Figure 9. The final output generated by the priority encoder for the 4-bit flash ADC is expressed in equations (2), (3), (4), and (5). This encoded digital output is then forwarded to the 4-bit digital-to-analog converter (DAC), which converts the digital value back into its corresponding analog representation.

$$B3 = D8 + D9 + D10 + D11 + D12 + D13 + D14 + D15 \quad (2)$$

$$B2 = D11' \times D10' \times D9' \times D8' (D4 \times D5 \times D6 \times D7) + D12 + D13 + D14 + D15 \quad (3)$$

$$B1 = D13' \times D12' \times D9' \times D8' (D5' \times D4' (D2' + D3') + D6 + D7) + D13 \times D12' (D10 + D11) + D14 + D15 \quad (4)$$

$$B0 = D14' \times D12' \times D10' \times D8' (D1' \times D2' \times D4' \times D6' + D6' \times D4' \times D3' \times D6' \times D5 + D7) + D14' \times D12' (D10' \times D9' \times D11) + D14' \times D13 + D15 \quad (5)$$

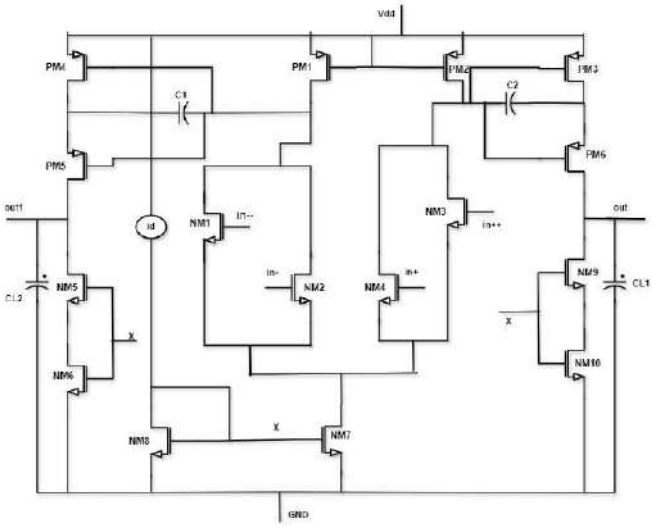

Figure 7.Schematic view of Comparator

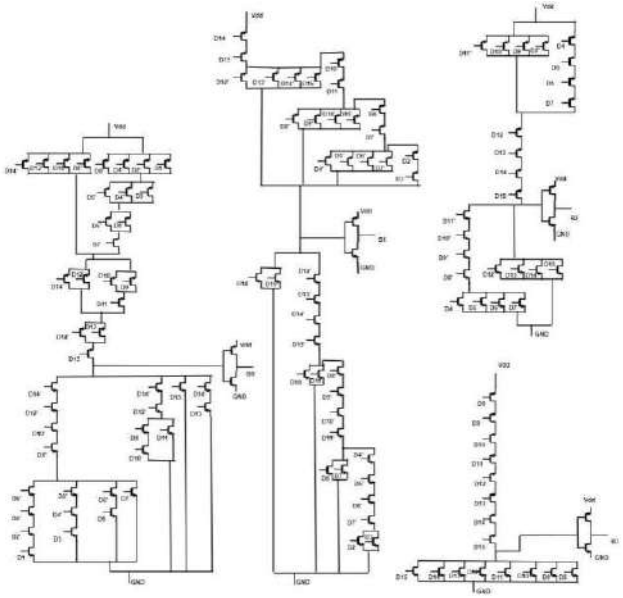

Figure 8.Schematic of Priority Encoder

II.D 4-Bit Digital to Analog Converter

The proposed 4-bit digital-to-analog converter (DAC) employs an inverting summing operational amplifier (Op-Amp) configuration, commonly used in binary-weighted resistor DACs. Here, the output voltage is obtained as the inverted summation of weighted input voltages. The resistor values at the input are set in binary-weighted ratios, such as 1R, 2R, 4R, and 8R, where each resistance is a multiple of 2. The corresponding output voltage is expressed as the weighted sum in equation (6):

$$V_{out}=-(V_a+V_b/2+V_c/4+V_d/8) \quad (6)$$

Where V_a represents the most significant bit (MSB) voltage and $V_d$corresponds to the least significant bit (LSB) voltage.

In the proposed design, a resistor value of 40 kΩ is selected to ensure accurate signal reconstruction. The schematic representation of the 4-bit DAC, utilized for converting the digital output of the flash ADC into its corresponding analog signal, is illustrated in Figure 10, while its transient response is presented in Figure 11.

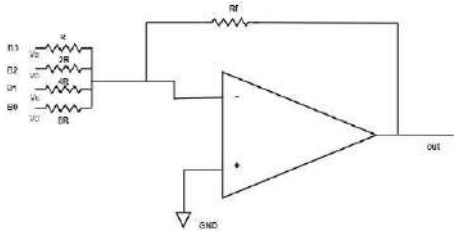

Figure 9.Schematic view of 4-Bit DAC

Performance analysis of the 4-bit DAC demonstrates precise correlation between digital inputs and corresponding analog outputs. The measured DNL and INL values of 0.4 LSB and -0.5 LSB respectively validate the conversion accuracy of the implemented architecture. Operating at a power consumption of 512.87 µW, the DAC achieves the desired resolution while maintaining power efficiency within the specified design constraints.The DAC output is subsequently subtracted from the S/H circuit output, and the resulting signal is fed into the residue amplifier, ensuring proper residue generation for the subsequent pipeline ADC stages.

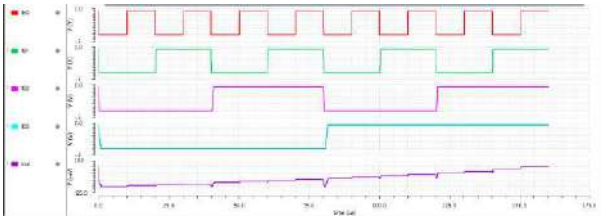

Figure 10.Simulation view of 4-Bit DAC

II.E Residue Amplifier

The residue amplifier, depicted in Figure 3, serves as a crucial gain stage within the pipeline ADC architecture. This amplification block compensates for signal attenuation by precisely boosting the residual voltage between stages, thereby maintaining optimal signal swing for subsequent quantization. The amplified residue undergoes further processing through the next-stage comparator network, ensuring preserved resolution throughout the pipelined conversion process. This interstage amplification mechanism directly influences the overall conversion accuracy of the cascaded architecture.

The proposed residue amplifier employs a fully differential architecture, featuring both differential inputs and differential outputs. This design enhances signal integrity and common-mode noise rejection, ensuring reliable performance in high-resolution ADC applications.

A folded cascode topology is utilized in the design, where the current path is redirected or "folded" using both NMOS and PMOS transistors. This topology combines the advantages of a cascode amplifier, such as high gain and reduced Miller effect (which improves bandwidth), with the simplicity and power efficiency of a single-stage amplifier. Due to its high-speed operation and superior bandwidth characteristics, folded cascode operational amplifiers are widely employed in high-speed ADC designs. The schematic of the folded cascode operational amplifier is illustrated in Figure 12.

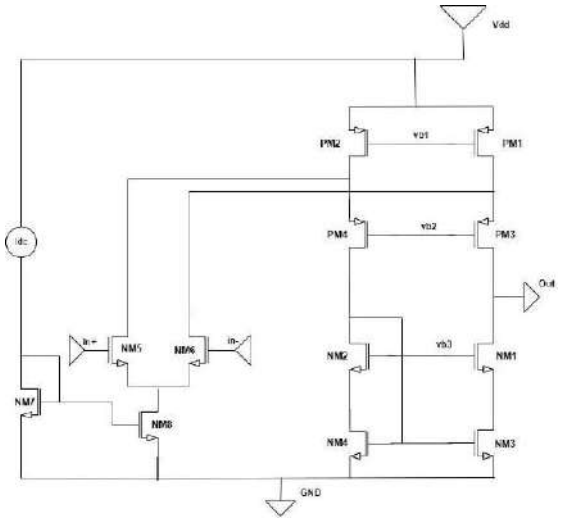

Figure 12.Schematic view of Folded Op-amp

II.D 4-DIGITAL CORRECTION LOGIC

In the proposed 20-bit pipeline ADC, the bit resolution process does not occur simultaneously across all stages. As a result, at different time instances, the output bits from each of the seven pipeline stages, corresponding to the same input sample, become available. To ensure correct timing alignment, a clocking system and simulation are employed to determine the required number of D flip-flops in each shift register, which subsequently selects the appropriate data.

Once the output bits from all seven stages are aligned, a digital correction process is performed. This correction method involves overlapping one bit from each stage with one bit from its neighboring stage, utilizing digital adders to ensure accurate data reconstruction. The schematic representation of the shift register and the 1-bit overlapping digital correction logic are illustrated in Figure 13 and Figure 14, respectively.

The final 20-bit output of the pipeline ADC is obtained by processing the shift register output through an adder, as depicted in Figure 15.

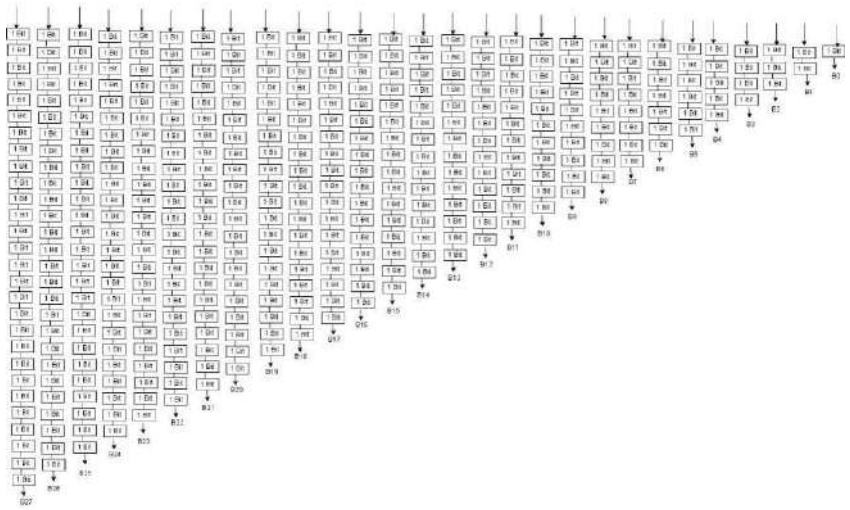

Figure 13.Schematic view of Shift Register

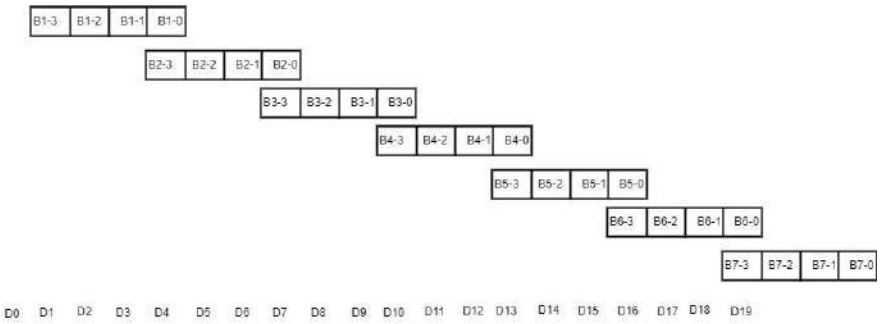

Figure 14.Schematic view of one bit Digital Correction Logic

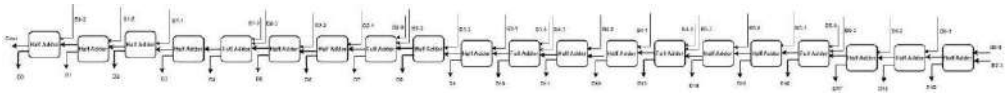

Figure 15.Schematic view of Adder for Digital Correction Logic

III. RESULT ANALYSIS

The proposed 20-bit pipeline ADC is simulated using 90nm CMOS technology with a 1.8 V supply voltage. The circuit simulation is performed for 53 cycles, determined using Equation (7):

$$N(\text{Number of cycles} = \frac{fin}{fs} \times 2^n \quad (7)$$

Where f_{in} is the input frequency, f_s is the sampling frequency, and n is the ADC resolution. The simulation results of the 20-bit pipeline ADC, sampled at 20 MS/s, are presented in Figure 16. The circuit exhibits an average power consumption of 16.7 mW, demonstrating its energy efficiency.

The FFT analysis, shown in Figure 17, is conducted at a 6 MHz sampling frequency. The ADC achieves an ENOB of 18.75, a SFDR of 154.57 dB, and a SNR of 114.69 dB, indicating excellent performance. The DNL results depicted in Figure 18, reveal a maximum DNL of +0.4 LSB and a minimum DNL of -0.18 LSB, ensuring high linearity.

Table 1 presents a quantitative comparison between the implemented 20-bit pipeline ADC and existing architectures from literature. The achieved sampling rate of 20 MS/s, coupled with enhanced resolution and power metrics, demonstrates notable performance advancement. This comparative analysis encompasses key performance indicators including conversion speed, effective resolution, and power efficiency. The measured results validate the architectural optimizations incorporated in this design, particularly in achieving higher throughput while maintaining power efficiency.

Table 1: Performance summary and comparison

Parameter	**proposed work**	**[1]**	**[3]**	**[4]**	**[5]**	**[6]**	**[7]**
Resolution(Bit)	**20**	12	08	9	10	10	10
Technology (nm)	**90**	180	180	65	180	65	180
Sampling Rate	**20 MS/s**	200 KS/s	500 KS/s	1 MS/s	1 KS/s	1 KS/s	120 KS/s
ENOB(bit)	**18.75**	10.62	7.5	-	7.2	8.53	9.34
SNR(dB)	**114.69**	65.59	46.92	53	45.90	53.13	58
SFDR (dB)	**154.57**	-	62.69	-	-	62.47	66
DNL (LSB)	**+0.4 -0.18**	2.68	+0.466 -0.66	+0.46 - 0.66	-	+0.46 - 0.95	0.77

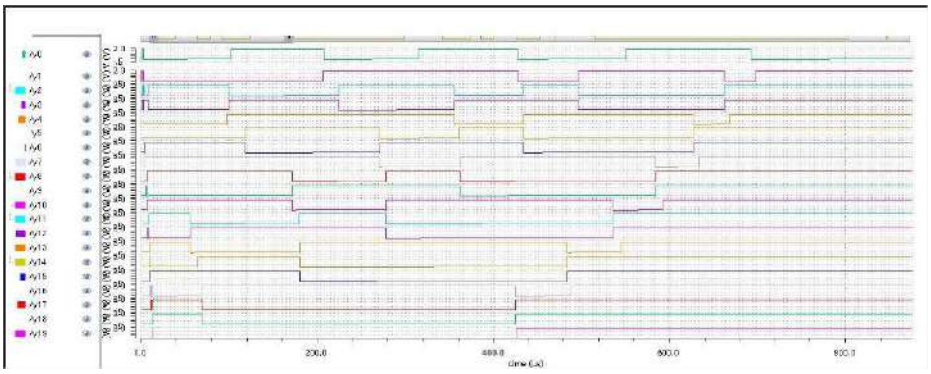

Figure 16.Simulation of Pipeline ADC

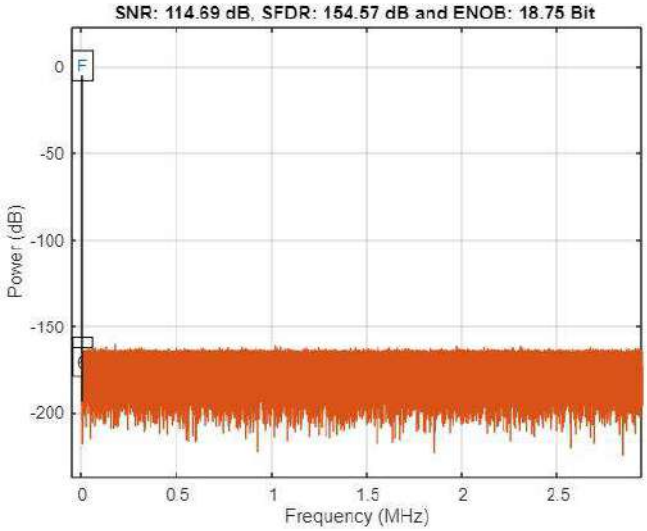

Figure 17 FFT Spectrum at sampling frequency of 6MHz

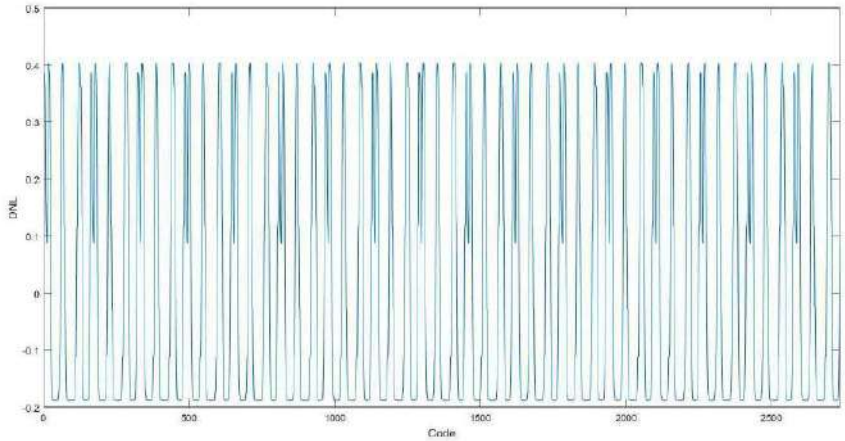

Figure 118 Measured DNL error

IV. CONCLUSION

This paper introduces innovative high-speed, high-resolution pipeline ADC architecture, designed with a 1.8V supply voltage and simulated using 90nm CMOS technology in Cadence. The proposed design achieves a 20-bit resolution with a sampling rate of 20 MS/s while maintaining an efficient power consumption of 16.7mW. The simulation results demonstrate significant improvements in performance metrics, particularly pertaining to SNR and SFDR. The proposed architecture achieves an SFDR and SNR enhancement of 46% and 49%, respectively, compared to [7]. These enhancements make the proposed ADC a highly suitable candidate for biomedical applications requiring high sampling rates and precision.

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